PCI Compliance of Altera Devices

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Introduction

The peripheral component interconnect (PCI) bus serves as a device-level interconnect for peripherals on a printed circuit board, and as a bus for high-performance expansion cards. The high performance of the PCI bus makes it a viable alternative to traditional bus architectures. The PCI bus architecture is ideal for applications such as network adapters, storage and embedded controllers, graphic accelerator boards, and audio-video products.

Altera MAX 7000, FLEX 8000, and FLASHlogic EPX8160 devices provide a programmable logic solution to a variety of PCI applications. This application brief shows how the pin requirements and device specifications for Altera MAX 7000, FLEX 8000, and EPX8160 devices satisfy PCI requirements. See Table 1.

Table 1. Summary of Altera PCI-Compliant Devices

PCI Specification		PCI Compliance		
Section	**Title**	**MAX 7000**	**FLEX 8000**	**EPX8160**
4.2	Component Specification	✓	✓	✓
4.2.1.1	DC Specifications	✓	✓	✓
4.2.1.2	AC Specifications	✓	✓	✓
4.2.3.1	Clock Specifications	✓	✓	✓
4.2.3.2	Timing Parameters	✓	✓	✓

This application brief should be used together with the following specification.

PCI Special Interest Group. ***PCI Local Bus Specification***. Rev. 2.0. Hillsboro, Oregon: PCI Special Interest Group, 1993.

Additional references are listed in *Recommended Reading* on page 9 in this application brief.

Go to *Application Note 41 (PCI Bus Applications in Altera Devices)* for more information on PCI applications. Go to the individual device data sheets in the Altera ***1995 Data Book*** for more information on Altera devices. Contact Altera Customer Marketing at (408) 894-7104 for information on device availability.

PCI Pin Definition

A minimum of 47 pins (for 32-bit bus operations) or 100 pins (for 64-bit bus operations) are required, as shown in Figure 2-1 in the ***PCI Local Bus Specification***. The Altera MAX 7000, FLEX 8000, and FLASHlogic devices shown in Table 2 can be used for 32-bit PCI applications; some can also be used for 64-bit PCI applications. Each Altera I/O pin can be tri-stated to provide Output Disable and bidirectional signal capabilities.

Table 2. Altera PCI-Compliant Devices

Device	Registers	Dedicated Inputs	User I/O Pins
EPM7032-7, EPM7032-6	32	4	32
EPM7064-7	64	4	64
EPM7096-7	96	4	72
EPM7128E-10P	128	4	96
EPM7160E-10P	160	4	100
EPM7192E-12P	192	4	120
EPM7256E-12P	256	4	160
EPF8282A-3, EPF8282A-2, *Note (1)*	282	4	74
EPF8452A-3, EPF8452A-2	452	4	116
EPF8636A-3, EPF8636A-2, *Note (1)*	636	4	132
EPF8820A-3, EPF8820A-2, *Note (1)*	820	4	148
EPF81188A-3, EPF81188A-2	1,188	4	180
EPF81500A-3, EPF81500A-2, *Note (1)*	1,500	4	204
EPX8160-10	160	48	120

Note:

(1) This device supports Joint Test Action Group (JTAG) boundary-scan testing (BST). The ***PCI Local Bus Specification*** recommends using five JTAG pins for BST.

PCI Electrical Specification

This section provides Altera device specifications and describes how they compare with PCI requirements. For your convenience, all headings in this section match section titles in the ***PCI Local Bus Specification***. For complete information on parameters, refer to the ***PCI Local Bus Specification***.

The following topics are discussed:

- 4.2 Component Specification
- 4.2.1.1 DC Specifications
- 4.2.1.2 AC Specifications
- 4.2.3.1 Clock Specification
- 4.2.3.2 Timing Parameters

4.2. Component Specification

The ***PCI Local Bus Specification*** recommends that devices operate within the commercial temperature range. All specifications listed for Altera devices are for a commercial range of V_{CC} = 5.0 V ± 5% and an ambient temperature (T_A) from 0° C to 70° C.

The ***PCI Local Bus Specification*** requires the availability of open-drain outputs. Altera devices have tri-state outputs that can emulate open-drain functionality.

4.2.1.1. DC Specifications

Table 3 shows the PCI DC specifications for 5.0-V devices and Altera device compliance with these specifications.

Table 3. PCI DC Specifications *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit	PCI Compliance		
						MAX 7000	FLEX 8000	EPX8160
V_{CC}	Supply voltage		4.75	5.25	V	✓	✓	✓
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.5	V	✓	✓	✓
V_{IL}	Low-level input voltage		–0.5	0.8	V	✓	✓	✓
I_{IH}	High-level input leakage current	*Note (2)*		70	µA	✓	✓	✓
I_{IL}	Low-level input leakage current	*Note (3)*		–70	µA	✓	✓	✓

Table 3. PCI DC Specifications *Note (1)*								
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**	**PCI Compliance**		
						MAX 7000	**FLEX 8000**	**EPX8160**
V_{OH}	High-level TTL output voltage	*Note (4)*	2.4		V	✓	✓	✓
V_{OL}	Low-level TTL output voltage	*Note (5)*		0.55	V	✓	✓	✓
C_{IN}	Input capacitance	*Note (6)*		20	pF	✓	✓	✓
L_{PIN}	Pin inductance			20	nH	✓	✓	✓

Notes to table:

(1) Specifications for PCI devices are from the ***PCI Local Bus Specification***.

(2) V_{IN} must be at least 2.7 V for PCI-compliant devices. V_{IN} equals V_{CC} for Altera devices.

(3) V_{IN} must be less than or equal to 0.5 V for PCI-compliant devices. V_{IN} equals GND for Altera devices.

(4) I_{OUT} must be less than or equal to –2 mA for PCI-compliant devices. I_{OUT} equals –4 mA for Altera devices.

(5) I_{OUT} must be at least 3 mA (for signals without pull-up resistors) and 6 mA (for signals with pull-up resistors) for PCI-compliant devices. I_{OUT} equals 8 mA for Altera devices.

(6) Refer to Section 4.1.2 of the ***PCI Local Bus Specification*** for system loading requirements. The maximum number of capacitive loads in the bus is 10. Expansion cards are allocated in 2 loads; PCI devices that are mounted directly on the motherboard are allocated in 1 load. Each load is 10 pF.

Altera devices can operate in a mixed 5.0-V/3.3-V power-supply environment, in which power pins for core logic operate at 5.0 V, and power pins for the I/O signals operate at 3.3 V. This dual-voltage capability is particularly useful when an Altera device drives a 3.3-V device.

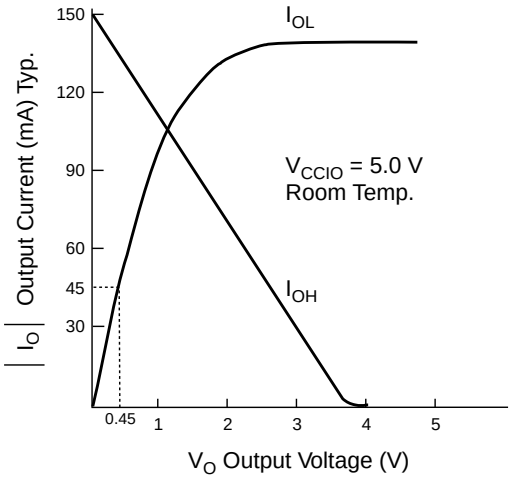
For information on power pins for core logic and power pins for I/O signals, go to the device family data sheets in the Altera ***1995 Data Book***.

4.2.1.2 AC Specifications

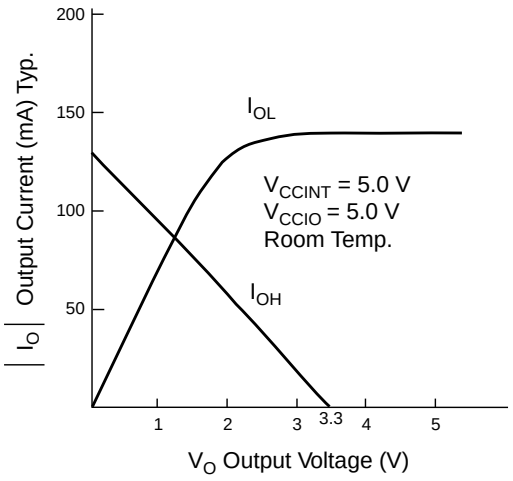
The ***PCI Local Bus Specification*** requires a device's output drive characteristics to be within a computed range, which is shown in Figure 4-3 in the ***PCI Local Bus Specification***. Figure 1 shows output drive characteristics for the MAX 7000, FLEX 8000, and FLASHlogic EPX8160 devices; these characteristics are within the PCI-specified range for V_{CC} and commercial temperatures.

Figure 1. MAX 7000, FLEX 8000 & EPX8160 Output Drive Characteristics

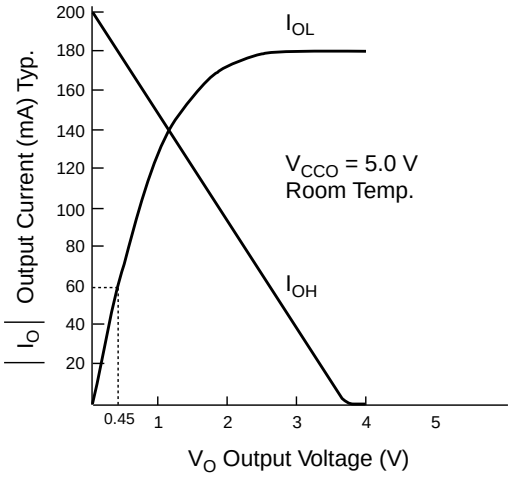
MAX 7000



FLEX 8000



EPX8160



The *PCI Local Bus Specification* lists three additional AC parameters, which are shown in Table 4. The minimum I_{CL} parameter ensures that devices are protected from voltage fluctuations. Altera devices include electrostatic discharge (ESD) protection circuits on all input and I/O pins. These circuits are designed to shunt high-voltage spikes to either the positive or negative power-supply circuits, preventing the high voltage from reaching internal circuits. Altera devices are tested and guaranteed to 1,500 V with a model that simulates electrostatic voltage pulses emitted by the human body. Devices also are tested and guaranteed to 200 V with a model that simulates voltage pulses emitted by machines.

Table 4. Additional PCI AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	PCI Compliance		
						MAX 7000	FLEX 8000	EPX8160
I_{CL}	Low clamp current	$-25 < V_{IN} \leq -1$	$\frac{-25 + (V_{IN} + 1)}{0.015}$		mA	✓	✓	✓
t_R	Unloaded output rise time	0.4 V – 2.4 V	1	5	V/ns	✓	✓	✓
t_F	Unloaded output fall time	2.4 V – 0.4 V	1	5	V/ns	✓	✓	✓

4.2.3.1. Clock Specification

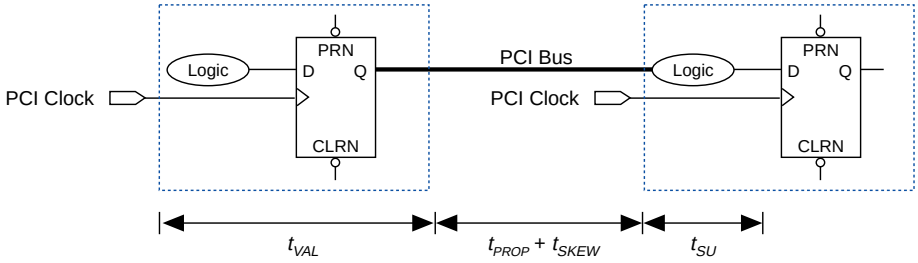
The PCI specification requires devices to support Clock frequencies up to 33 MHz (t_{CYC} = 30 ns), as shown in Table 5. However, timing parameters can be increased for applications with frequencies less than 33 MHz.

Table 5. PCI Clock Specifications

Symbol	Parameter	Min	Max	Unit	PCI Compliance		
					MAX 7000	FLEX 8000	EPX8160
t_{CYC}	Clock cycle time	30		ns	✓	✓	✓
t_{HIGH}	Clock high time	12		ns	✓	✓	✓
t_{LOW}	Clock low time	12		ns	✓	✓	✓
–	Clock slew rate	1	4	V/ns	✓	✓	✓

The Clock cycle time is analyzed in four segments, as shown in Figure 2. A PCI device must meet the t_{VAL} and t_{SU} timing parameters. A PCI design must meet the total Clock skew (t_{SKEW}) and bus propagation time (t_{PROP}). For 33-MHz operation, the total value for all timing parameters must provide a minimum Clock period of 30 ns. Specific details on PCI and Altera device timing parameters are provided in 4.2.3.2. Timing Parameters below.

Figure 2. PCI Clock Cycle Path



The t_{SKEW} and t_{PROP} values for 33-MHz and 25-MHz PCI buses are the same. Only t_{VAL} and t_{SU} can be increased for 25-MHz operation.

4.2.3.2. Timing Parameters

The key PCI timing parameters for the MAX 7000, FLEX 8000, and FLASHlogic EPX8160 devices are shown in Table 6.

Table 6. PCI Timing Parameters

Symbol	Parameter	Min	Max	Unit	PCI Compliance		
					MAX 7000	FLEX 8000	EPX8160
t_{VAL}	Clock to signal valid delay—bus signals, *Note (1)*	2	11	ns	✓	✓ *(2)*	✓
$t_{VAL(PTP)}$	Clock to signal valid delay—point to point, *Note (1)*	2	12	ns	✓	✓	✓
t_{ON}	Float to active delay	2		ns	✓	✓	✓
t_{OFF}	Active to float delay		28	ns	✓	✓	✓
t_{SU}	Input setup time to Clock—bus signals	7 *Note (3)*		ns	✓	✓	✓
$t_{SU(PTP)}$	Input setup time to Clock—point to point	10, 12 *Note (3)*		ns	✓	✓	✓
t_H	Input hold time from Clock		0	ns	✓	✓ *(4)*	✓

Notes:

(1) Minimum values are measured with 0-pF equivalent load; maximum values are measured with 50-pF equivalent load. Actual test capacitance may vary.

(2) In FLEX 8000 devices, registers that are near I/O pins and I/O cell registers meet the specification $t_{CO} = 11$. Use the MAX+PLUS II Timing Analyzer to verify timing for specific devices.

(3) This timing parameter is measured for applications that run at 33 MHz. It can be increased for applications that run at speeds slower than 33 MHz.

(4) To meet $t_H = 0$ for core registers in FLEX 8000 devices, data signals should enter the device through the column pins.

MAX 7000 devices comply with the PCI t_{VAL} timing parameters. The setup time for MAX 7000E devices with a –10P or –12P speed grade meets the
7-ns timing specification for a 33-MHz PCI system. For lower-frequency applications, an 8-ns or 10-ns setup time may be sufficient.

The FLEX 8000 timing parameters are measured using signals that are driven out by the I/O element (IOE) registers. Logic functions are implemented with core logic elements (LEs) and then driven to the IOE registers. The t_{VAL} value is identical for all I/O pins because the register is on the periphery of the device; t_{SU} varies by up to 4 ns depending on pin and LE placement. FLEX 8000A devices are faster than the equivalent FLEX 8000 devices; the t_{VAL} time for I/O cell registers in FLEX 8000A devices is 9.2 ns, which meets the 11-ns t_{VAL} requirement.

The EPX8160-10 device complies with all PCI timing requirements.

Conclusion

Altera's MAX 7000, FLEX 8000, and EPX8160 FLASHlogic devices provide a programmable logic solution for the growing number of PCI bus applications by satisfying the following requirements:

- *DC Specifications*—Altera devices meet the PCI current and voltage specifications. Surface-mount package options should be used if pin capacitance and inductance are important to the board design.
- *AC Specifications*—Altera PCI-compatible devices comply with the PCI AC specifications.
- *Timing Parameters*—MAX 7000 devices with –7, –10P , and –12P speed grades, all FLEX 8000A devices, and the EPX8160 FLASHlogic device meet the PCI timing parameters for 33-MHz operation.

Recommended Reading

Altera recommends reading the documentation contained in the PCI Development Kit, available from Altera's Literature Department. In addition, the following documents are available from the PCI Special Interest Group. To purchase a copy, call (800) 433-5177 (U.S.) or (503) 797-4207 (all other locations).

- ***PCI Local Bus Specification, Revision 2.0***
- ***PCI BIOS Specification***
- ***System Design Guide***
- ***Multi-Media Design Guide***
- ***PCI to PCI Bridge***

The following book is available from technical bookstores:

Shanley, Tom, and Don Anderson. ***PCI System Architecture***. Richardson, Texas: MindShare, Inc., 1994.

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